In the Claims:

The claims are as follows:

1-79. (canceled)

80. (Original) A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

81. (Original) The method of making the multi-layered interconnect structure of claim 80 wherein said step of positioning said first and second dielectric layers on said first and second

opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 °F.

82. (Previously Amended) The method of making the multi-layered interconnect structure of claim 80 wherein said positioning said first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, comprises the steps of:

laminating a first copper foil and a second copper foil respectively onto said first and second dielectric layers; and

etching selected portions of said first and second copper foils to respectively produce first and second pluralities of said electrically conductive members.

83. (Original) The method of making the multi-layered interconnect structure of claim 80 further including the steps of:

positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members;

removing portions of said third dielectric layer to expose portions of said first plurality of electrically conductive members; and

forming a first plurality of microvias within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

84. (Original) The method of making the multi-layered interconnect structure of claim 83

wherein said removing of said portions of said third dielectric layer is performed by laser ablating.

85. (Original) The method of making the multi-layered interconnect structure of claim 80 further including the steps of:

positioning a fourth dielectric layer on said second dielectric layer and on said second plurality of electrically conductive members;

removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and

forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

86. (Original) The method of making the multi-layered interconnect structure of claim 85 wherein the step of removing portions of said fourth dielectric layer is performed by laser ablating.

87. (Original) A method of making an electronic package comprising the steps of:

providing a semiconductor chip having a first surface including a plurality of contact sites thereon;

providing a multi-layered interconnect structure adapted for electrically interconnecting said semiconductor chip to a circuitized substrate, said multi-layered interconnect structure including a thermally conductive layer, having first and second opposing surfaces, first and

second dielectric layers positioned on said first and second opposing surfaces, respectively, and first and second pluralities of electrically conductive members positioned on said first and second dielectric layers, respectively;

providing a first plurality of solder connections on said first plurality of electrically conductive members; and

connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact sites on said semiconductor chip, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip.

88. (Previously Amended) The method of making the electronic package of claim 87 further comprising positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members, wherein said step of providing said first plurality of solder connections on said first plurality of electrically conductive members includes:

forming a plurality of openings in said third dielectric layer, each of said openings including an internal wall and exposing a portion of at least one of said first plurality of electrically conductive members;

plating a conductive layer on said internal wall of said plurality of openings and on said exposed portion of said at least one of said first plurality of electrically conductive members to define a plurality of microvias;

applying a first solder paste onto said conductive layer; and

reflowing said solder paste to form a first plurality of solder connections.

89. (Original) The method of making the electronic package of claim 88 wherein said step of connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact members on said semiconductor chip further includes the steps of applying a second solder paste onto said respective ones of said first plurality of solder connections, positioning said respective ones of said contact members of said semiconductor chip against said respective ones of said first plurality of solder connections, and reflowing said second solder paste and said respective ones of said first plurality of solder connections to electrically connect said semiconductor chip to said multi-layered interconnect structure.

90. (Original) The method of making the electronic package of claim 87 further including the steps of:

providing a circuitized substrate having a first surface including a plurality of contact pads thereon;

providing a second plurality of solder connections on said second plurality of conductive members of said multi-layered interconnect structure; and

connecting respective ones of said second plurality of said solder connections to respective ones of said plurality of contact pads on said circuitized substrate to make electrical connections therebetween.

91. (Original) A method of making a multi-layered interconnect structure adapted for electrically

interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively;

positioning a first electrically conductive layer within said first dielectric layer;

positioning a second electrically conductive layer between said first electrically conductive layer and said thermally conductive layer wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

92. (Original) The method of making the multi-layered interconnect structure of claim 91 wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of

from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F.

93. (Original) The method of making the multi-layered interconnect structure of claim 91 wherein said positioning said first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, comprises the steps of:

laminating a copper foil onto said first and second dielectric layers; and

etching selected portions of said copper foil to produce first and second pluralities of said electrically conductive members.

94. (Original) The method of making the multi-layered interconnect structure of claim 91 further including the steps of:

positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members;

removing portions of said third dielectric layer to expose portions of said first plurality of electrically conductive members; and

forming a first plurality of microvias within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

95. (Original) The method of making the multi-layered interconnect structure of claim 94 wherein said removing of said portions of said third dielectric layer is performed by laser ablating.

96. (Original) The method of making the multi-layered interconnect structure of claim 91 further including the steps of:

positioning a fourth dielectric layer on said second dielectric layer and on said second plurality of electrically conductive members;

removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and

forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

97. (Original) The method of making the multi-layered interconnect structure of claim 96 wherein the step of removing portions of said fourth dielectric layer is performed by laser ablating.